Single Electron Tunneling Device Based Computation

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Presentation Overview

- Introduction
- Single Electron Tunneling Devices
- Single Electron Encoded Logic
- Electron Counting
- Delay Insensitive Circuits
- Conclusions
Introduction

- Processing power of logic and arithmetic circuit has increased dramatically since the invention of the transistor.
- Moore’s “law” (1965) states that processing power doubles every 18 months.
- Why did this work for the last four decades?
  - Advances in algorithms and device technology.
  - Feature sizes reduction and hence increase in number of transistor per cm².

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Present and Near Future

- Current primary technology: (C)MOS
  - 90 nm, 65 nm, 45 nm, ...
  - Forecast: in 10 years physical gate lengths below 10 nm.
  - Predictions were (sometime) proved wrong in the past but ...
- Alternative (candidate) technologies:
  - Single Electron Tunneling (SET),
  - Rapid Single Flux Quantum (RSFQ),
  - Resonant Tunneling Diodes (RTD),
  - Magnetic and Electron Spin Devices,
  - Carbon Nanotubes,
  - ….

Present and Near Future

- Facts
  - Sooner or later MOS transistor feature size scaling ends.
  - As-of-yet it is not known which technology, if any, will succeed CMOS.
- Issues
  - Complexity
  - Unpredictability (variability)
  - Reliability
  - Behavior
  - Communication
- Required
  - Design Methodologies
  - Computation Paradigms
  - Architectures
  - Programming Models
Novel Nano Devices

- (C)MOS successor desirable characteristics include:
  - Greater feature size scaling potential than (C)MOS.
  - Extremely low power consumption.
  - Potential to operate at room temperature.
  - Sufficiently fast processing speed when used in conjunction with appropriate design techniques and architectures.

- Single Electron Tunneling (SET)
  - Simple device structure.
  - Single electron “currents”.
  - Technology independent.

Why SET?

- Tunneling is a behavior.
- Tunnel junctions can be manufactured in different technologies such as:
  - Conventional lithography,
  - Patterned oxide deposition,
  - Carbon nanotubes.
Single Electron Tunneling

- Basic circuit element:
  - (quantum) Tunnel Junction - two (metal) conductors separated by an insulator.
  - “leaking capacitor”, such that the leaking can be controlled by the voltage across the junction.

Orthodox Switching Model

- Critical Voltage:
  \[ V_c = \frac{q_e}{2(C_s + C_i)} \]

- Switching Delay:
  \[ t_d = -\ln(P_{error}) \frac{q_e R_i}{|V| - V_c} \]

- Energy Consumption:
  \[ \Delta E = q_e (|V| - V_c) \]

We assume \( P_{error} = 10^{-8} \).
State of the Art

- Main focus - device fabrication.

- Circuit
  - Mimic the behavior of the MOS transistor
    - Delay: $O(100^+)$ electrons tunnel per switching event
    - Power: Large designs have leakage currents.
  - Multiple Tunnel Junction (MTJ)
    - Switch by transporting one electron only.
    - No leakage current.
    - Require complicated control logic with three voltage levels.

Electron Trap

- Can control the transport of individual electrons.
- Electrons are transported one at a time.
- The less transported, the faster the circuit!
Our Way

Goal:
- Design circuit with charge transport of one electron only and no leakage currents.

Strategy:
- Focus on SET specific behavior.
- Exploit the SET ability to transport individual electrons.
- Avoid mimicking existing CMOS design styles.
- Use the relation between Tunnel Junction and Threshold Logic.

Assumptions:
- The thermal tunneling/co-tunneling error probability of is less than $P_{error}$.
- Neglect random background charge.

Research lines:
- Single Electron Encoded Logic (SEEL).
- Electron Counting (EC).
- Delay Insensitive Circuits (DIC).

Single Electron Encoded Logic

- Represent bits by single electrons
  - ‘0’ = 0 electron
  - ‘1’ = 1 electron

Logic gate removes 1 electron from the output node if result is Boolean ‘1’.

$$V_{out} = \frac{-q_e}{C} \quad V_{out} = \frac{1.602e^{-19}(C)}{10e^{-18}(F)} = 16mV$$

Typically $C$ is 10 aF.
Threshold Logic

- An n-input linear Threshold Logic Gate (TLG) can compute any linearly separable Boolean function given by:

\[ F(X) = \text{sgn}(\mathcal{F}(X)) = \begin{cases} 0 & \text{if } \mathcal{F}(X) < 0 \\ 1 & \text{if } \mathcal{F}(X) \geq 0 \end{cases} \]

\[ \mathcal{F}(X) = \sum_{i=1}^{n} \omega_i x_i - \theta \]

- A single n-input TLG can compute an n-input AND, OR, NAND or NOR function as follows:

\[ \text{AND}(a_1, a_2, \ldots, a_n) = \text{sgn}\{a_1 + a_2 + \ldots + a_n - n\} \]

\[ \text{OR}(a_1, a_2, \ldots, a_n) = \text{sgn}\{a_1 + a_2 + \ldots + a_n - 1\} \]

\[ \text{NAND}(a_1, a_2, \ldots, a_n) = \text{sgn}\{-a_1 - a_2 - \ldots - a_n + n - 1\} \]

\[ \text{NOR}(a_1, a_2, \ldots, a_n) = \text{sgn}\{-a_1 - a_2 - \ldots - a_n\} \]

SEEL Linear Threshold Gate

**How to construct a threshold gate:**
- Start with an electron box circuit.
- Bias \( V_j \) around \( V_c \) with bias voltage \( V_b \).
- Inputs \( V^p \) add to \( V_j \).
- Inputs \( V^n \) subtract from \( V_j \).

**Result**
- When \( V_j > V_c \) the output is ‘high’.
- \( V_o \) act as threshold adjuster.

**Formally**
\[
\begin{align*}
C^p &= \sum (C^p + C_o) \\
C^n &= \sum (C^m_n + C_o) \\
V_o &= \text{sgn}(V_j - V_c) = \text{sgn}\{\mathcal{f}(X)\} \\
\mathcal{f}(X) &= C^p \sum V^p_i C^p_i + C^n \sum V^n_i C^n_i - \psi \\
\psi &= 0.5 (C^p + C^n) e - C^m_n C_o V_b
\end{align*}
\]
SEEL Threshold Gates

- **AND gate**
  \[ a \text{ AND } b = \text{SGN}\{a + b - 2\} \]
- **OR gate**
  \[ a \text{ OR } b = \text{SGN}\{a + b - 1\} \]
- **Full Adder SUM gate**
  \[ S_i = \text{sgn}\{a_i + b_i + c_{i+1} - 2c_{i-1}\} \]

SEEL Networks

- SEEL TLG operate correctly as stand-alone gates.
- As network components fan-out related feedback and feed forward effects occur.
- Two types of feedback occur:
  - Static feedback from bias voltages.
  - Dynamic feedback from switching activity.
- Static feedback can be compensated by adjusting the TLG circuit parameters.
- Dynamic feedback can be considered as “random” and cannot be compensated through the adjustment of circuit parameters.

**Solution:**
- Augment passive logic gates with an output buffer consisting of two SET transistors.
- Add bias capacitors to implement an inverting buffer.
SEEL Network Example

Gates consisting of logic gate combined with buffer.

Circuit Diagram

Simulation Results

Truth Table

Electron Counting Paradigm

Basic Principle: Represent values by number of electrons.

Specific building blocks are required!
Move k electron (MVke) Block

When enabled (re)moves $V^*k$ electrons (from) to a reservoir.

4-bit Digital to Analog Converter

- Requires 4 MVke blocks.
Periodic Symmetric Function

- Can evaluate a PSF function characterized by $a$, $b$, and $T$.
- PSF functions important for many arithmetic functions such as parity and counting.
- The electron trap circuit displays periodic behavior.

PSF Block Implementation

- A SET inverter is used to implement a literal function such that
  - $F_p = '0'$ if $V_{out\ (trap)} > 0$
  - $F_p = '1'$ if $V_{out\ (trap)} < 0$
5-bit Analog to Digital Converter

- Requires 5 PSF blocks.

Electron Counting Addition

- A and B are converted to the charge encoded representation.
- By utilizing a common charge reservoir for A and B the addition operation is implemented at no additional costs.
- The charge encoded representation of A+B is reconverted to binary by n+1 PSF blocks.
- Adding two n-bit operands requires a depth-2 network composed of 3n+1 EC components (Mvke and PSF block).
- The addition scheme can be utilized to implement parity, multi-operand addition and n/log n counting functions.
Electron Counting Multiplication

- B is converted to the charge encoded representation.
- The charge encoded value B serves as input V, the input bits $a_i$ are used as enable (E) signals.
- The charge encoded representation of A·B is reconverted to binary by n+1 PSF blocks.
- Multiplying two n-bit operands requires a depth-3 composed of 4n EC components.

... another way?

- Synchronous computations in SET:
  - Unknown delays => error correction required
  - Required clock area
  - Clock skew
  - Physical variations
- Avoid synchronous issues
  - Delay Insensitive Circuits
  - Brownian Circuits
- Universal set of circuit primitives
  - NAND-gate in clocked circuits
  - Token-based circuits: *non-clocked*
Signal Representation

- Less carriers to represent signal
- Token-based circuits
- Noise and Fluctuations

Our Approach

- No clock: wires more local, less heat dissipation
- Delay-insensitive circuits: robust to signal delays
- Brownian motion of signals: allow... and, exploit!

How to exploit noise?

Search in space through Brownian Motion

Similarly, state space of circuit can be searched
Brownian Motion Circuits

- Random charge transport in SET
- Utilize signal fluctuations
- Search through Brownian maze
- No deadlock
- Universal set:
  - Hub
  - Conservative Join

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Universal set of circuit primitives

Hub

CJoin
Hub

Hub Simulation

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Conservative Join

CJ Simulation
Brownian Circuit Example

BN Simulation 1
BN Simulation 2

Half-Adder
BN Example: Half-adder

Half-adder Simulation
Conclusions

- Single Electron Encoded Logic family
  - Threshold Gate
  - Buffered Gates
  - Networks
  - Memory Elements
- Electron Counting Paradigm.
  - Specific Basic Building Blocks
  - Algorithms: Addition, Multiplication, Division
- Delay Insensitive Circuits
- Brownian Circuits

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